CLAIMS

What is claimed is:

1. A computer system comprising:

a central processing unit (CPU); and

a cache memory, coupled to the CPU, having a plurality of compressible cache lines to store additional data.

2. The computer system of claim 1 wherein the computer system further comprises a cache controller to perform lookup operations of the cache memory.

3. The computer system of claim 1 wherein the cache controller is included within the CPU.

4. The computer system of claim 2 wherein the cache controller comprises an array of tags corresponding to each of the plurality of cache lines, each tag having one or more compression encoding bits indicating whether a corresponding cache line is compressed.

5. The computer system of claim 4 wherein a single cache line stores two or more cache lines if the corresponding compression bit indicates that the line is compressed.

6. The computer system of claim 4 wherein each tag includes one or more companion encoding bits indicating which companion lines are stored in a

common cache set.

7. The computer system of claim 5 wherein the companion lines are adjacent memory lines.

8. The computer system of claim 4 wherein the companion encoding bits used as a compression format bit to select between different compression algorithms.

9. The computer system of claim 4 wherein the companion encoding bits used to encode the ordering of companion lines in the compressed line.

10. The computer system of claim 6 wherein the cache controller further comprises set and way selection logic to select a cache line.

11. The computer system of claim 10 wherein the set and way selection logic comprises tag comparison logic to compare a cache line address to tags in the arrays of tags.

12. The computer system of claim 11 wherein the tag comparison logic ignores the one or more companion encoding bits within the address if the one or more compression encoding bits indicate that the cache line is compressed.

13. The computer system of claim 11 wherein the tag comparison logic compares the one or more companion bits within the address with the one or

more companion encoding bits within the tag if the compression encoding bits indicate that the cache line is not compressed.

14. The computer system of claim 10 wherein the cache controller further comprises compression logic to compress a cache line.

15. The computer system of claim 14 wherein the compression logic compresses cache lines via a dictionary based compression algorithm.

16. The computer system of claim 14 wherein the compression logic compresses cache lines via a sign-bit compression algorithm.

17. The computer system of claim 14 wherein the compression logic determines when a cache line is to be compressed.

18. The computer system of claim 17 wherein the compression logic compresses a cache line based upon opportunistic compression.

19. The computer system of claim 17 wherein the compression logic compresses a cache line based upon prefetch compression.

20. The computer system of claim 17 wherein the compression logic compresses a cache line based upon victim compression.

21. The computer system of claim 14 wherein the cache controller further

comprises byte selection logic to select addressed datum within a cache line.

22. The computer system of claim 21 wherein the byte selection logic comprises:

a decompressor to decompress a selected cache line;

an input multiplexer to select between a decompressed cache line and an un-decompressed cache line; and

an output multiplexer to select between companion lines in the uncompressed cache line.

23. A cache controller comprising:

compression logic to compress lines within a cache memory device; and

set and way logic to select cache lines.

24. The cache controller of claim 23 further comprising an array of tags corresponding to each of the cache lines, each tag having one or more compression encoding bits indicating whether a corresponding cache line is compressed.

25. The cache controller of claim 24 wherein a single cache line stores two or more cache lines if the corresponding compression bit indicates that the line is compressed.

26. The cache controller of claim 24 wherein each tag includes one or more companion encoding bits indicating which companion lines are stored in a common cache set.

27. The cache controller of claim 26 wherein the set and way selection logic comprises tag comparison logic to compare a cache line address to tags in the arrays of tags.

28. The cache controller of claim 27 wherein the tag comparison logic ignores the one ore more companion encoding bits within the address if the one or more compression encoding bits indicate that the cache line is compressed.

29. The cache controller of claim 28 wherein the tag comparison logic compares the one ore more companion bits within the address with the one ore more companion encoding bits within the tag if the compression encoding bits indicates that the cache line is not compressed.

30. The cache controller of claim 23 wherein the compression logic compresses cache lines via a dictionary based compression algorithm.

31. The cache controller of claim 23 wherein the compression logic compresses cache lines via a sign-bit compression algorithm.

32. The cache controller of claim 23 wherein the compression logic determines

when a cache line is to be compressed.

33. The cache controller of claim 23 wherein the cache controller further comprises byte selection logic to select addressed datum within a cache line.

34. The cache controller of claim 33 wherein the byte selection logic comprises:

a decompressor to decompress a selected cache line;

an input multiplexer to select between a decompressed cache line and an un-decompressed cache line; and

an output multiplexer to select between companion lines in the uncompressed cache line.

35. A method comprising:

determining if a first cache line within a cache memory device is to be compressed; and

compressing the first cache line.

36. The method of claim 35 wherein compressing the first cache line comprises storing data from a second cache line within the first cache line.

37. The method of claim 35 further comprising analyzing a tag associated with the first cache line in a tag array to determine if the first cache line is

compressed.

38. The method of claim 37 further comprising analyzing one or more companion encoding bits if the first cache line is not compressed.

39. The method of claim 38 further comprising disregarding the one or more companion encoding bits if the first cache line is compressed.

40. The method of claim 37 further comprising using the one or more companion encoding bits as a compression format bit to select between different compression algorithms if the first cache line is compressed.

41. The method of claim 37 further comprising using the one or more companion encoding bits to encode the ordering of companion lines in the first cache line if the first cache line is compressed.

42. A computer system comprising:

a central processing unit (CPU);

a cache memory, coupled to the CPU, having a plurality of compressible cache lines to store additional data;

a chipset coupled to the CPU; and

a main memory.

43. The computer system of claim 1 wherein the computer system further

comprises a cache controller to perform lookup operations of the cache memory.

44. The computer system of claim 1 wherein the cache controller is included within the CPU.

45. The computer system of claim 1 wherein the cache controller is included within the chipset.

46. The computer system of claim 43 wherein the cache controller comprises an array of tags corresponding to each of the plurality of cache lines, each tag having one or more compression encoding bits indicating whether a corresponding cache line is compressed.

47. The computer system of claim 46 wherein a single cache line stores two or more cache lines if the corresponding compression bit indicates that the line is compressed.